

661FX-M

Rev: A

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Revision History :

1. Ver A: Initial
2. Ver B:
 - (1) Add North Bridge Fan Sink Header
 - (2) Delete SATA Crystal
 - (3) Modify USB, AUDIO, S/P DIF Out, Front Panel Headers for ACER
 - (4) Add SATA Status LED Signal via Front Panel
 - (5) Modify USB Power Source on South Bridge due to SiS AP note
 - (6) Add One More Fuse for 1394 Header
 - (7) Add SPDIF02 Header (Pitch 2.0mm) for HP S/P DIF Out
 - (8) Modify Hardware Reset Circuit
 - (9) Modify VCCVID Power Good Circuit
 - (10) Remove IR, SIRQ Headers
 - (11) Add JP4, JP5 Headers for HP
 - (12) Modify CPU Fan Control Circuit
 - (13) Change RT9173 for DDR Vtt
 - (14) Change LAN Connector Type
3. Ver 1.0:
 - (1) Add C289, MC40 for EMI Solution

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4. Socket478-1
5. Socket478-2
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8. SiS661FX-2 (Memory)
9. SiS661FX-3 (VGA / HyperZip)
10. SiS661FX-4 (Power)
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12. SiS964-2 (Misc. Signals)
13. SiS964-3 (USB)
14. SiS964-4 (Power)
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20. VGA / IDE Connectors
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30. HM/FAN/RING/LPC
31. Voltage Regulator
32. DUAL 5V, 3V& SB Regulator
33. VRD10 (CPU Vcore)
34. ATX / Panel / RTC

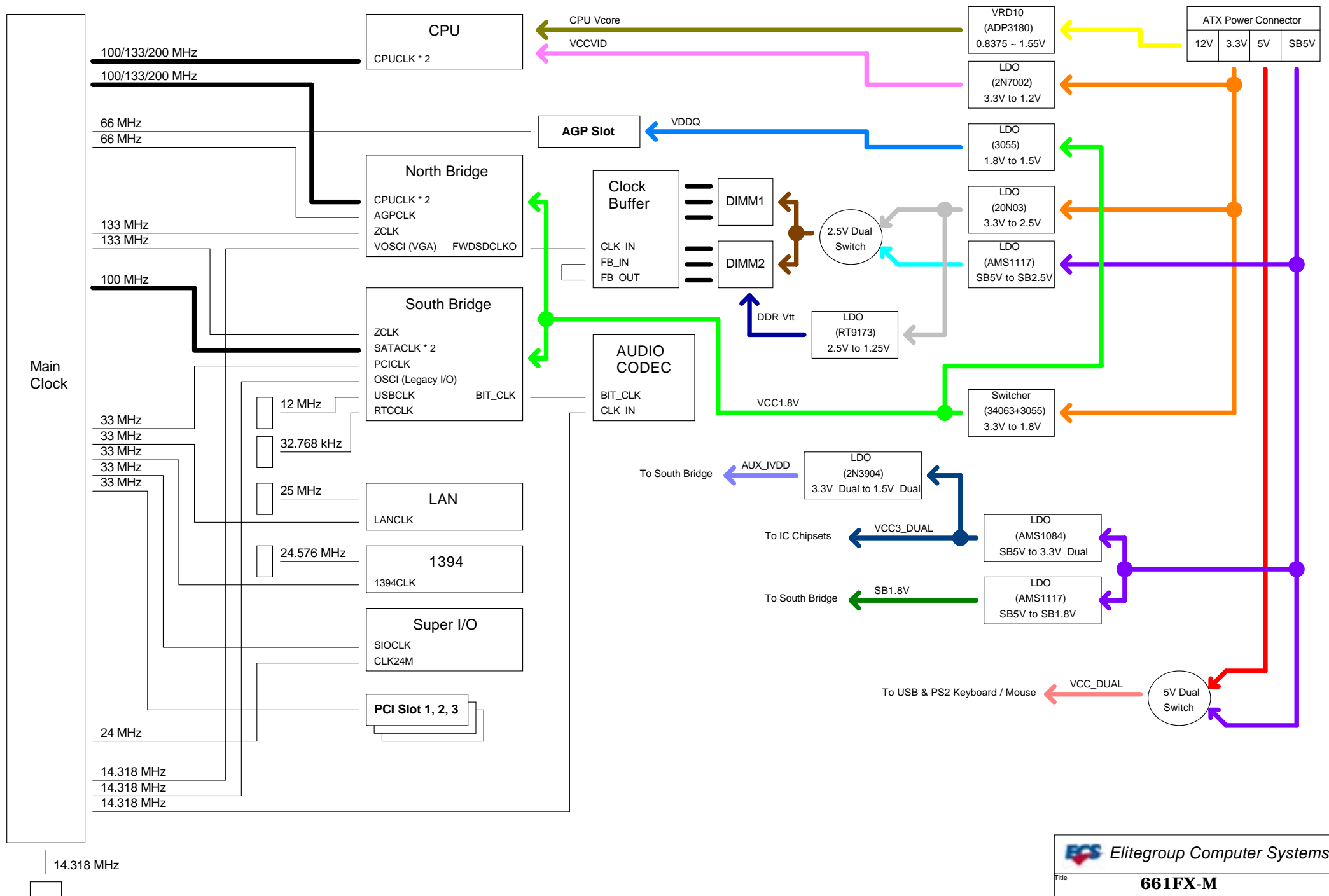


	SIGNATURE	DATE
DESIGNER		
LAYOUT		
CHECK		
APPROVAL		

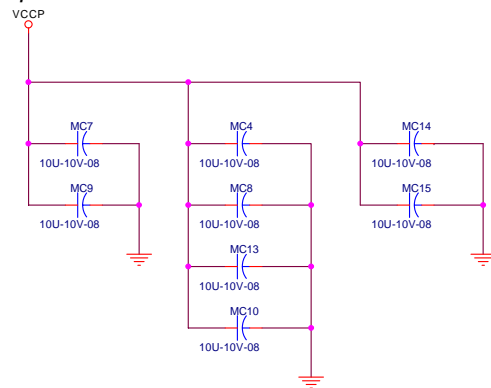


Elitegroup Computer Systems

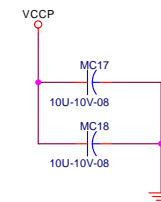
File		661FX-M		Rev	A
Size	Document Number	Cover Sheet			
Custom					
Date	Monday, September 22, 2003	Sheet	1	of	34



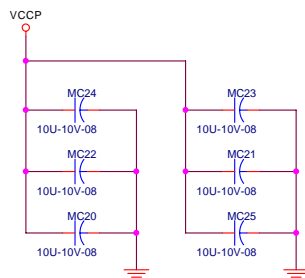
Put these capacitors at processor NORTH SIDE



Put these capacitors INSIDE PROCESSOR CAVITY

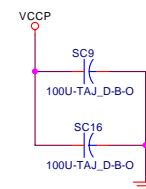


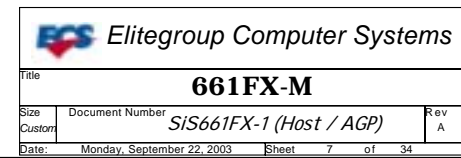
Put these capacitors at processor SOUTH SIDE

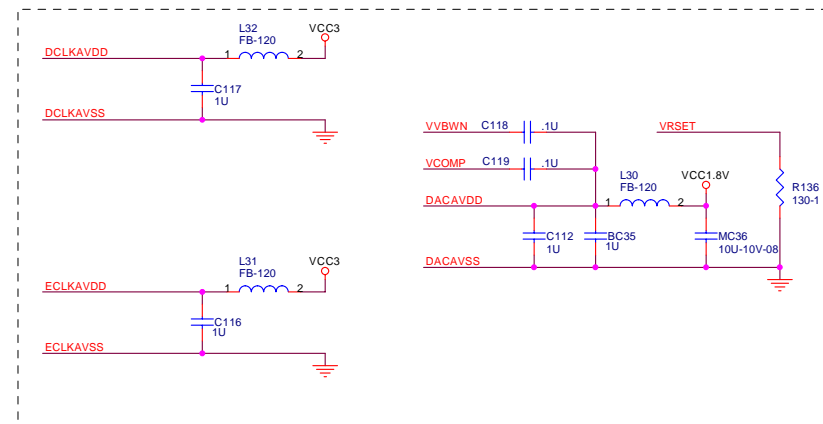


P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.

Put these capacitors at processor SOLDER SIDE





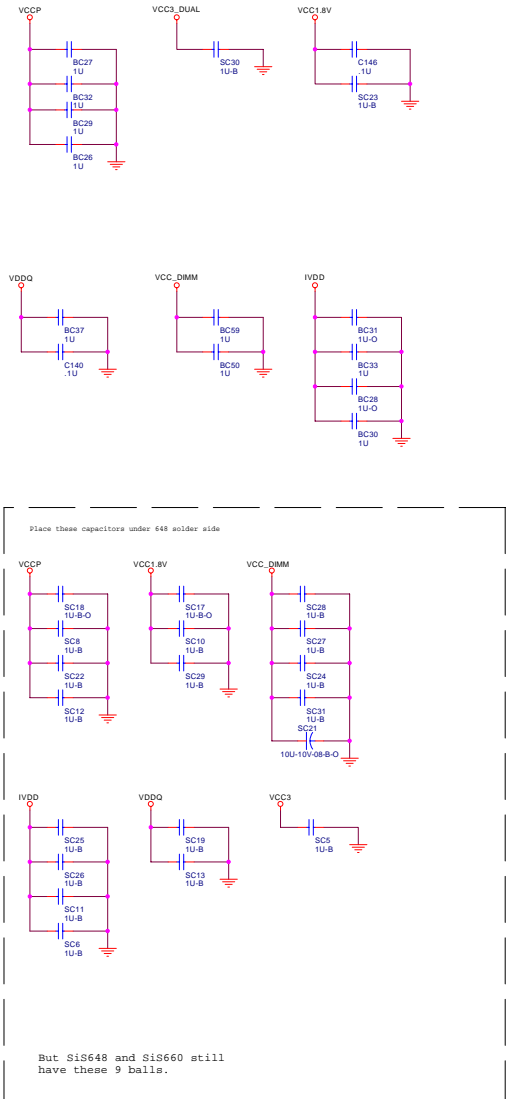


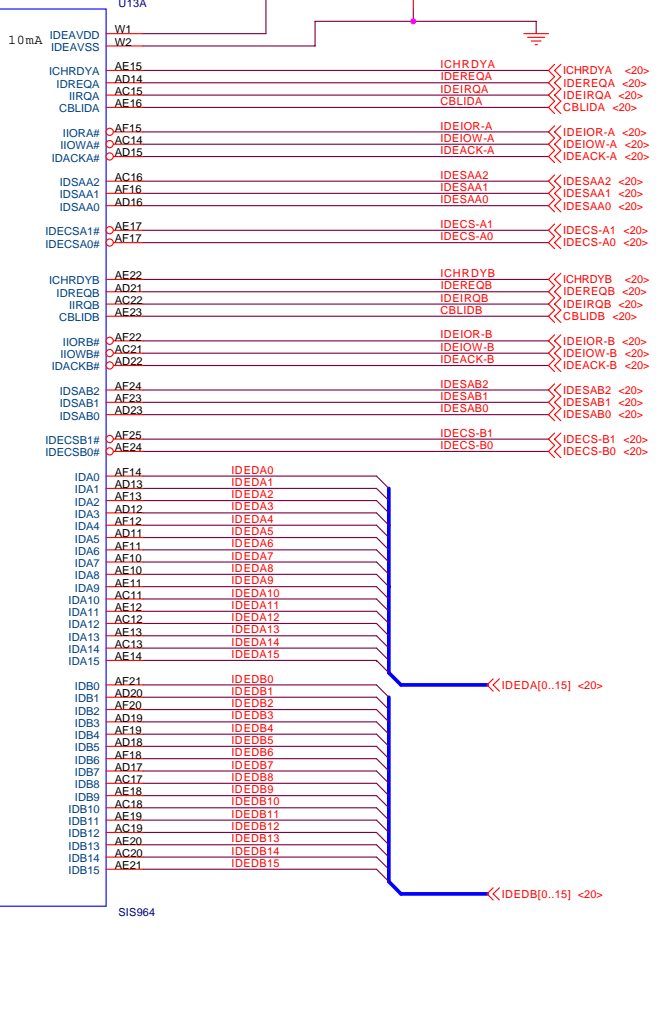
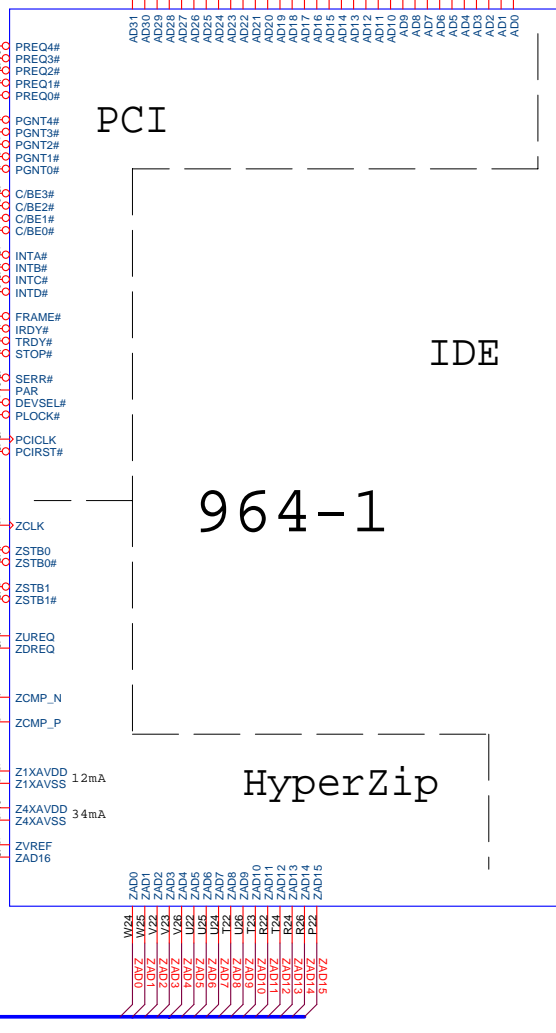
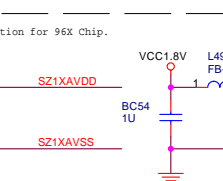
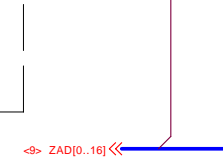
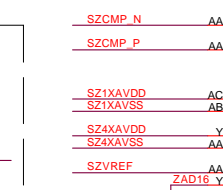
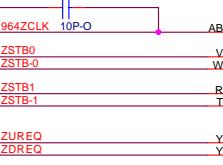
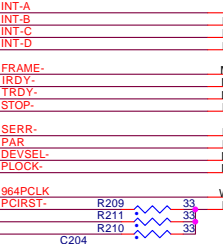
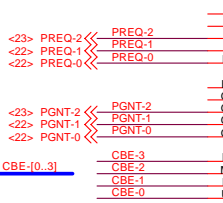
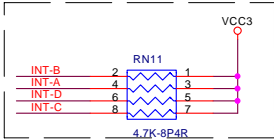
661FX-4

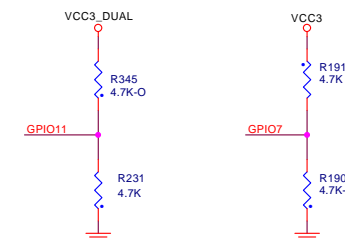
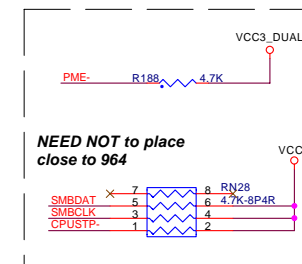
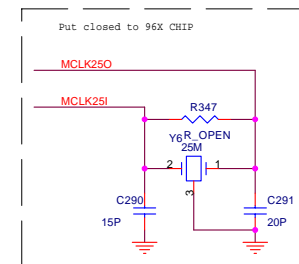
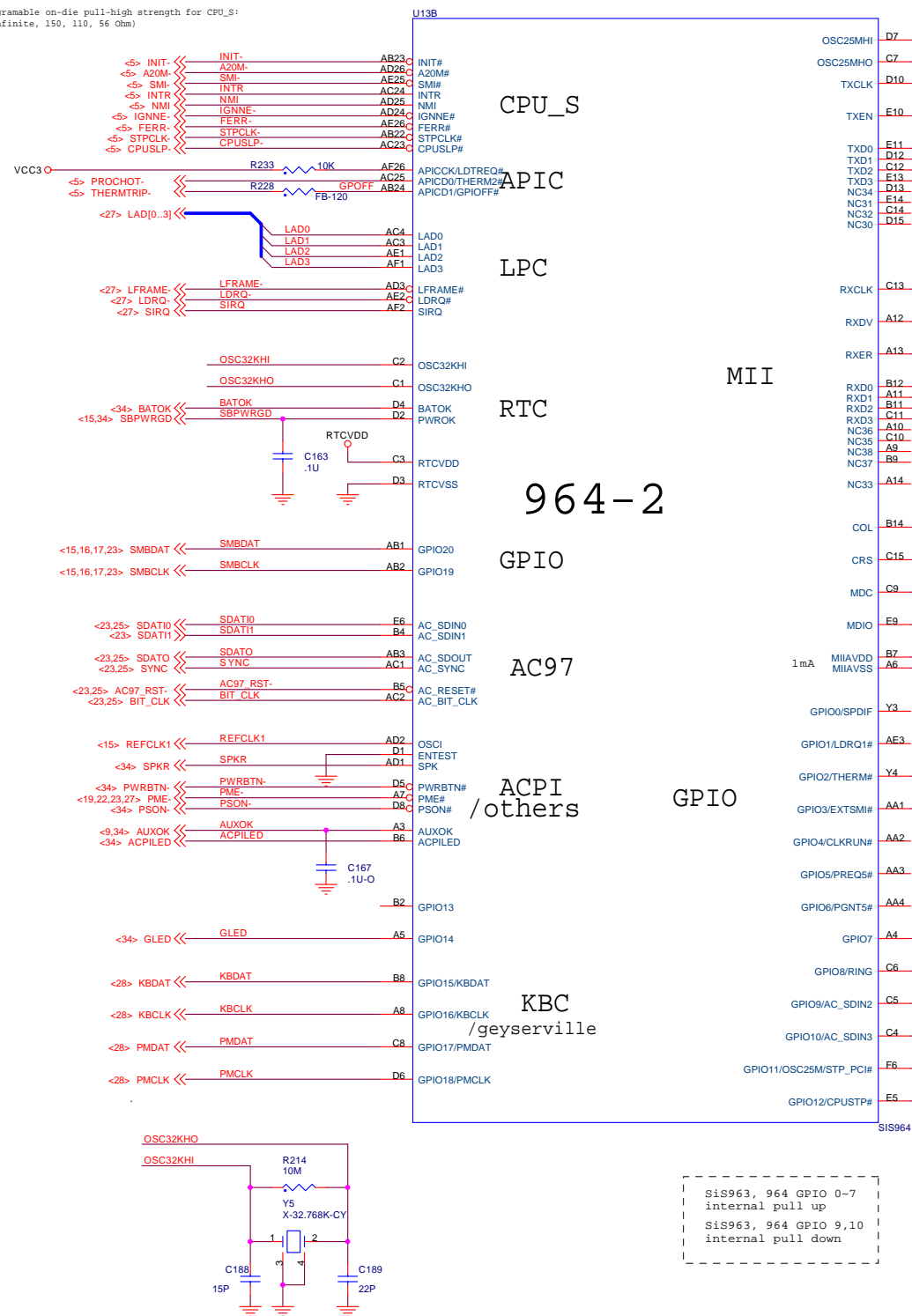
Power

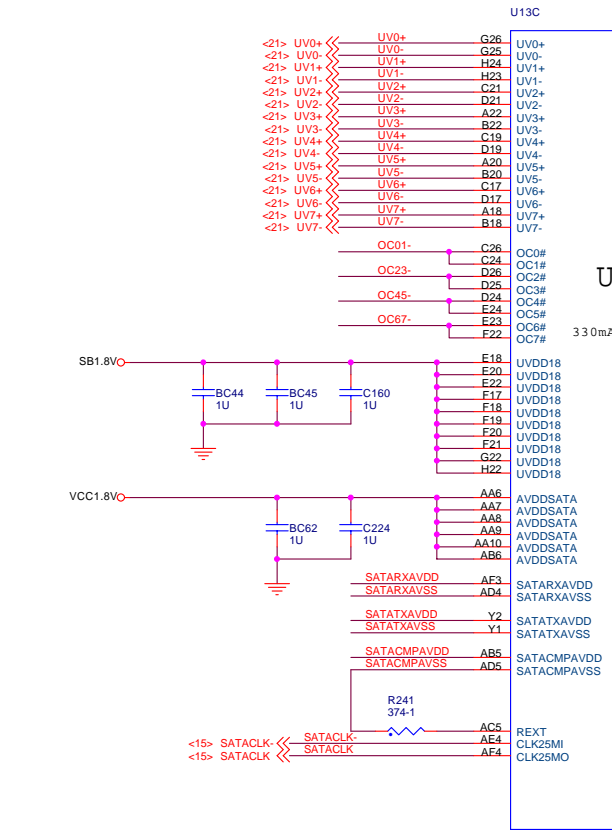
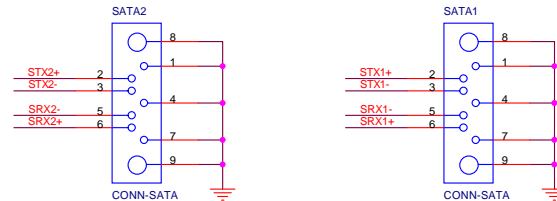
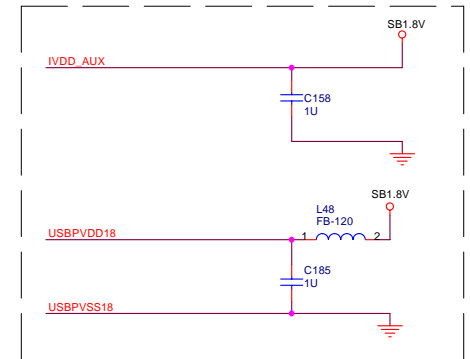
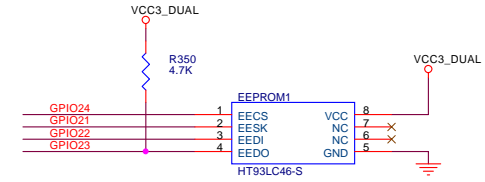
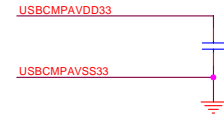
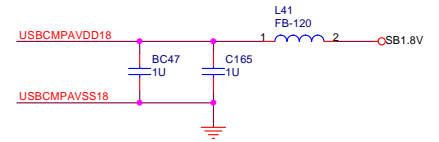
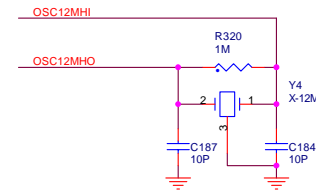
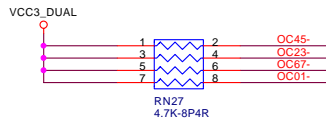
NOTE:
SiS648FX doesn't have
the following 9 balls
VDDQ(P12), VDDM(AE14), VDDM(AE15),
VDDM(AB25), IVDD(N20), IVDD(T24),
VTT(M20), VTT(N25), VTT(P25).

AUX_IVDD=10.12mA
AUX3.3=26.38mA

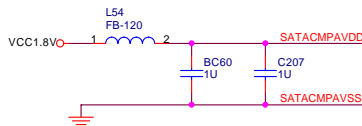
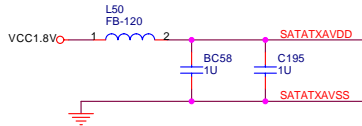
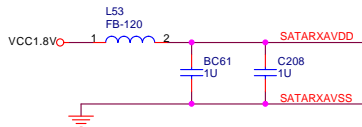


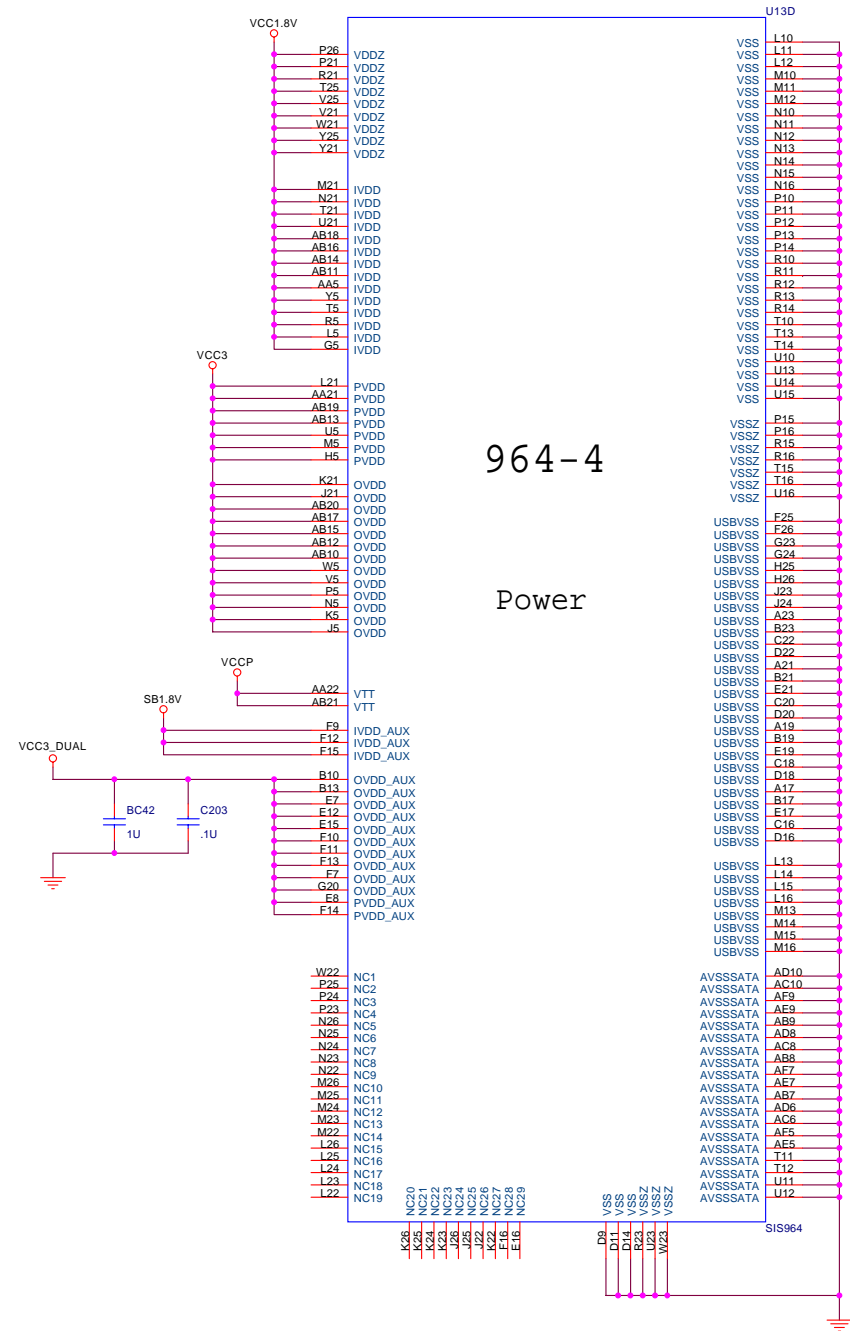
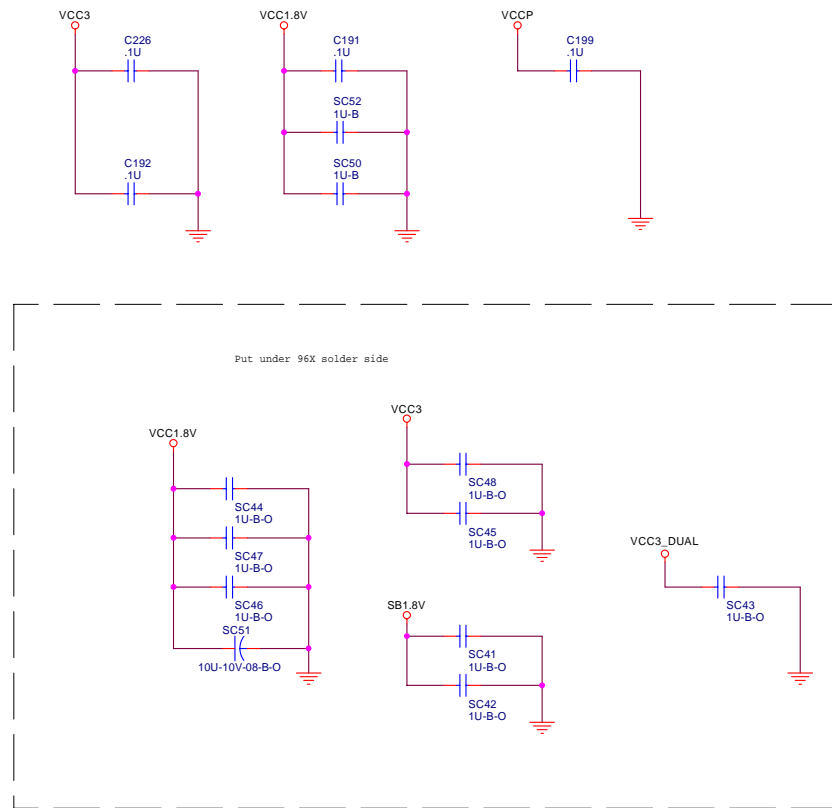




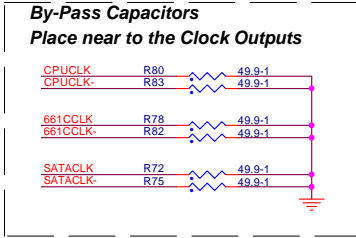
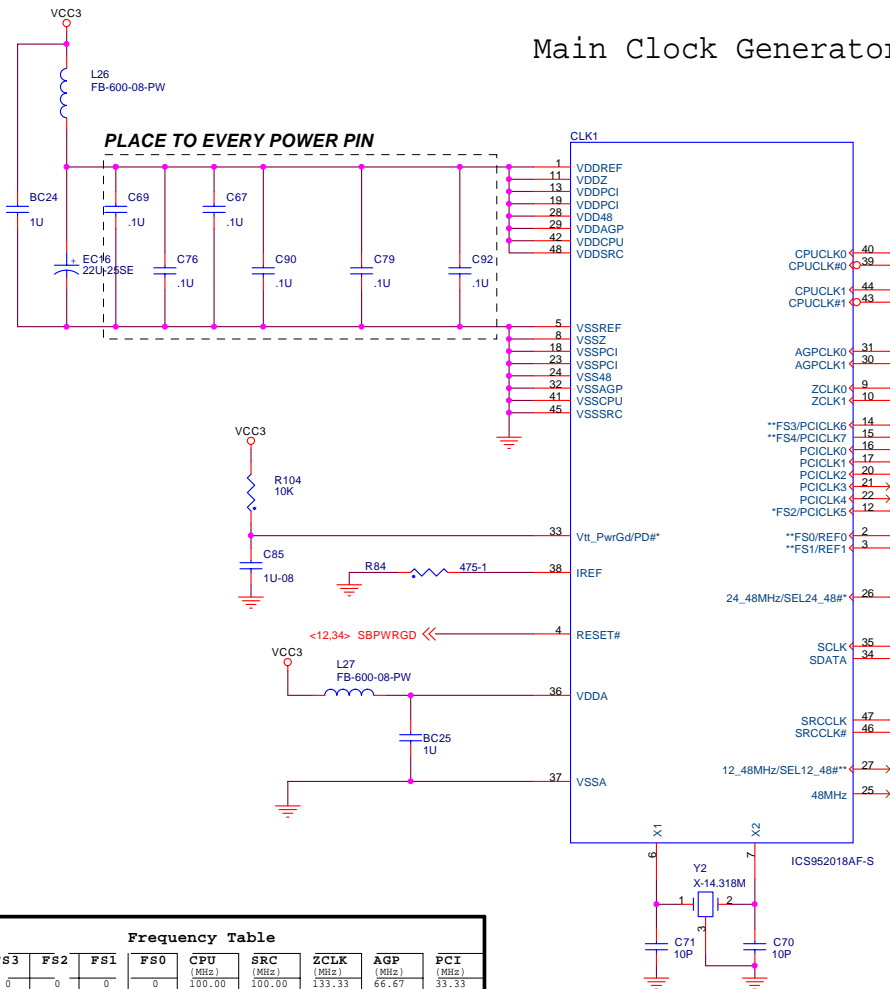


964-3





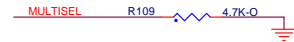
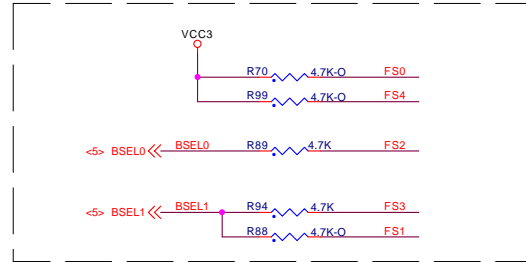
Main Clock Generator



	FS4	FS3	FS2	FS1	FS0	CPU	SRC	ZCLK	AGP	PCI
FSB400	0	0	0	0	0	100.00	100.00	133.33	66.67	33.33
FSB533	0	0	0	0	1	100.99	100.99	134.65	67.33	33.66
FSB800	0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
	0	0	1	0	0	133.33	100.00	133.33	66.66	33.33
	0	0	1	0	1	134.65	100.99	134.65	67.32	33.66
	0	0	1	1	0	137.33	103.00	137.33	68.66	34.33
	0	0	1	1	1	133.33	100.00	133.33	66.67	33.33
	0	1	0	0	0	200.00	100.00	133.33	66.67	33.33
	0	1	0	0	1	201.98	100.99	134.65	67.33	33.66
	0	1	0	1	0	206.00	103.00	137.33	68.67	34.33
	0	1	0	1	1	200.00	100.00	133.33	66.67	33.33
	0	1	1	0	0	166.66	125.00	125.00	66.66	33.33
	0	1	1	0	1	168.31	126.23	126.23	67.32	33.66
	0	1	1	1	0	171.66	128.74	128.74	68.66	34.33
	0	1	1	1	1	166.66	125.00	125.00	66.66	33.33

	FS4	FS3	FS2	FS1	FS0	CPU	SRC	ZCLK	AGP	PCI
1	1	0	0	0	0	105.00	105.00	140.00	70.00	35.00
1	1	0	0	0	1	107.00	107.00	142.67	71.33	35.67
1	1	0	0	1	0	109.00	109.00	145.33	72.67	36.33
1	1	0	0	1	1	110.00	110.00	146.67	73.33	36.67
1	1	0	1	0	0	140.00	105.00	140.00	70.00	35.00
1	1	0	1	0	1	142.66	107.00	142.67	71.33	35.67
1	1	0	1	1	0	145.33	109.00	145.33	72.66	36.33
1	1	0	1	1	1	146.66	110.00	146.66	73.33	36.67
1	1	1	0	0	0	210.00	105.00	140.00	70.00	35.00
1	1	1	0	0	1	214.00	107.00	142.67	71.33	35.67
1	1	1	0	1	0	218.00	109.00	145.33	72.67	36.33
1	1	1	0	1	1	220.00	110.00	146.67	73.33	36.67
1	1	1	1	0	0	266.66	100.00	133.33	66.67	33.33
1	1	1	1	0	1	269.33	101.00	134.67	67.33	33.67
1	1	1	1	1	0	274.66	103.00	137.33	68.67	34.33
1	1	1	1	1	1	266.66	100.00	133.33	66.67	33.33

Frequency Selection

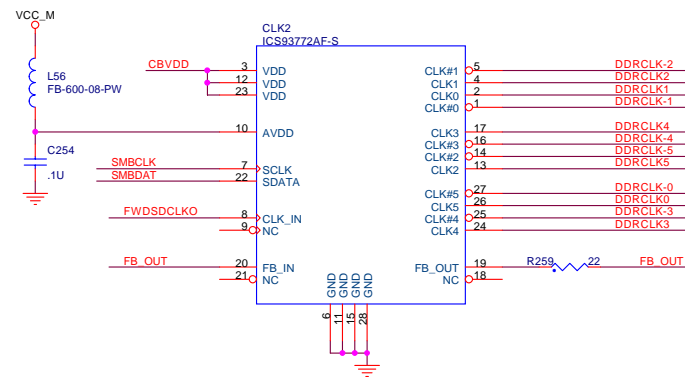
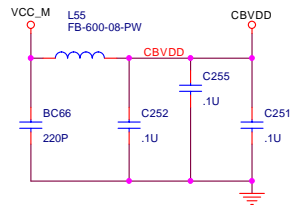


Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	BSEL1	BSEL0	Low	Low
CPU=100 (BSEL[1:0]=00)	0	0	0	0	0
CPU=133 (BSEL[1:0]=01)	0	0	1	0	0
CPU=200 (BSEL[1:0]=10)	0	1	0	0	0

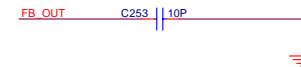
Clock Buffer (DDR)

(5 OPTIONS)
 1: (ICS) ICS93716
 2: (Winbond)
 3: (ICWorks)
 4: (IMI)
 5: (AMI)

By-Pass Capacitors
 Place near to the Clock Buffer



DDRCLK[0..5] <<DDRCLK[0..5] <17>
 DDRCLK[0..5] <<DDRCLK[0..5] <17>
 SMBCLK <<SMBCLK <12,15,17,23>
 SMBDAT <<SMBDAT <12,15,17,23>
 FWDSCLKO <<FWDSCLKO <8>

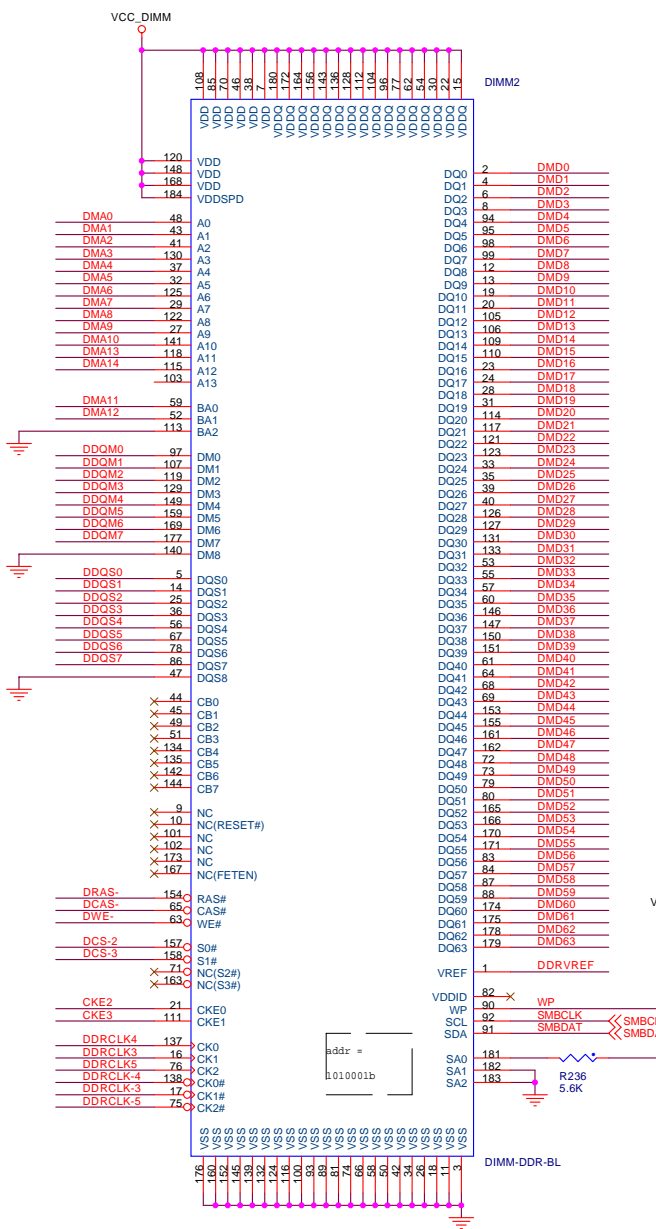
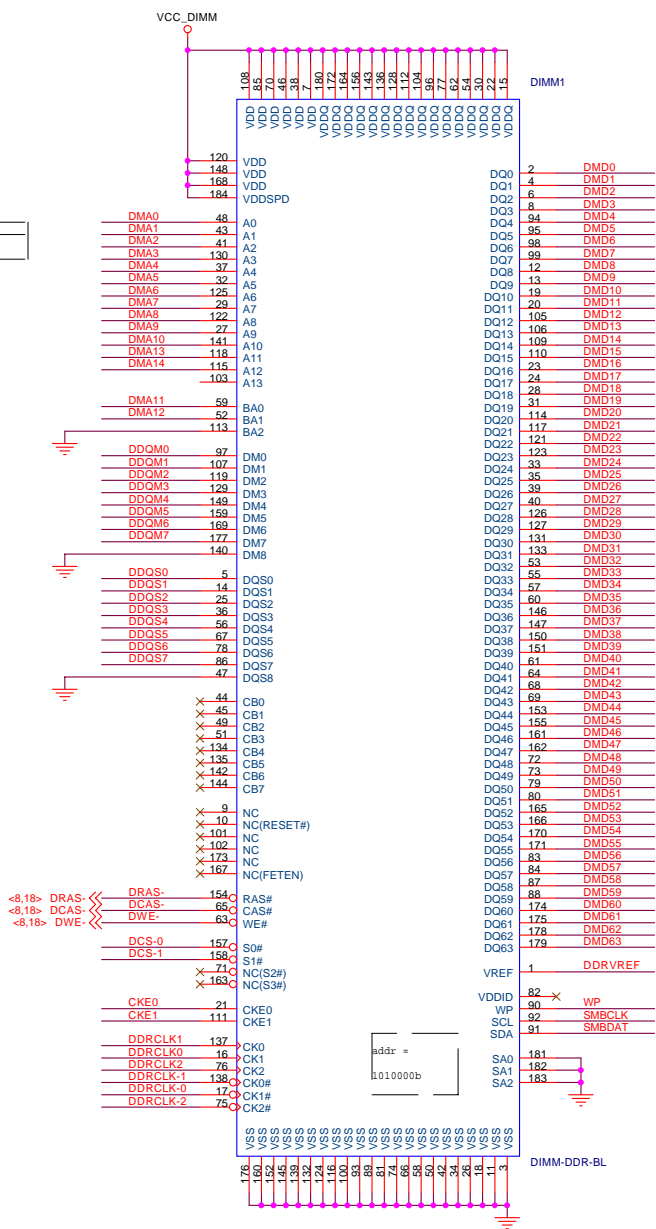


NOTE:
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

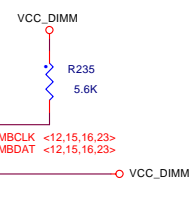
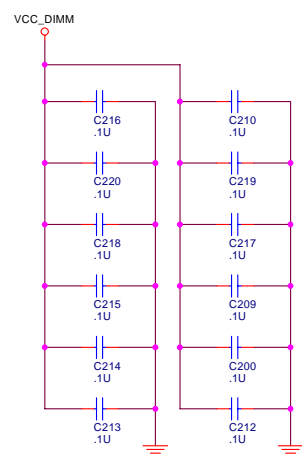
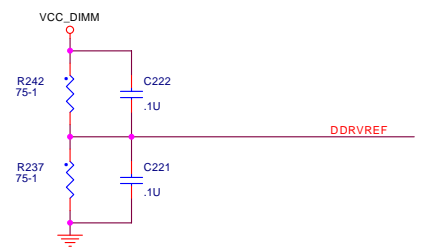
VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7



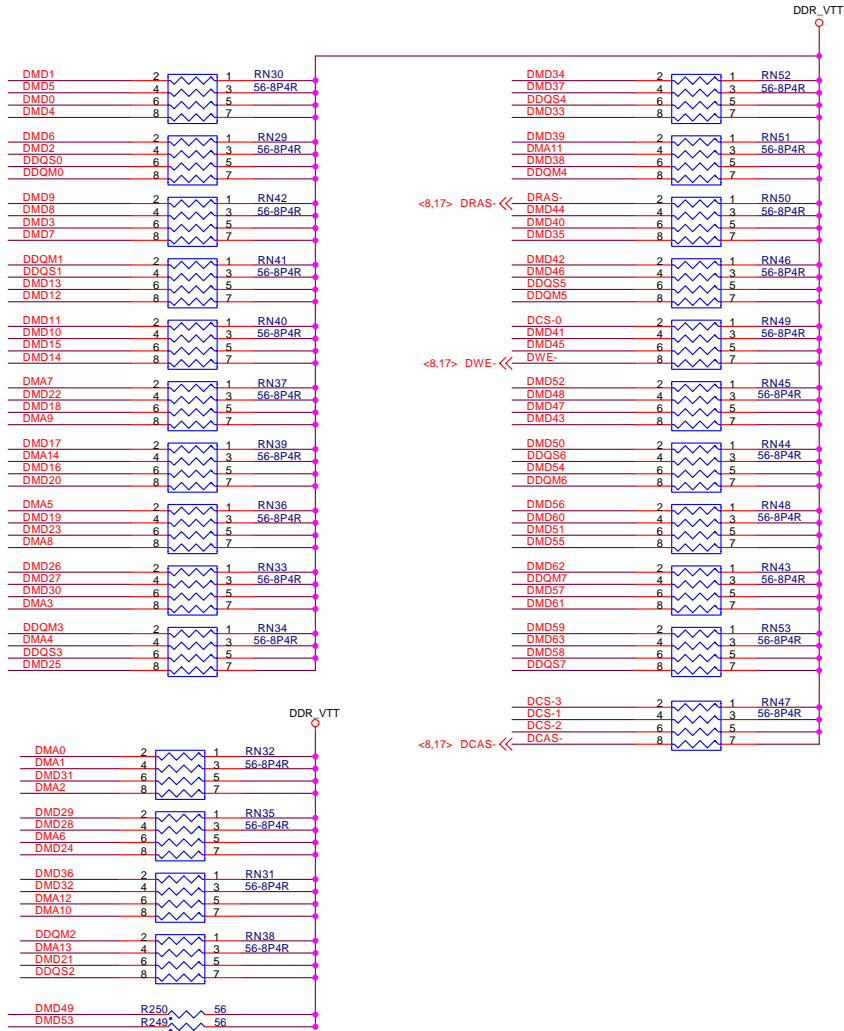
- DMD[0..63] << DMD[0..63] <8,18>
- DMA[0..14] << DMA[0..14] <8,18>
- DDQM[0..7] << DDQM[0..7] <8,18>
- DDQS[0..7] << DDQS[0..7] <8,18>
- DCS[0..3] << DCS[0..3] <8,18>
- CKE[0..3] << CKE[0..3] <8>
- DDRCLK[0..5] << DDRCLK[0..5] <16>
- DDRCLK[0..5] << DDRCLK[0..5] <16>



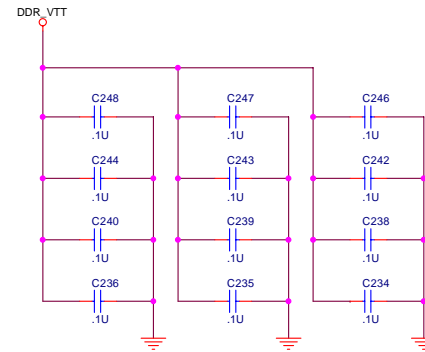
SSTL-2 Termination Resistors

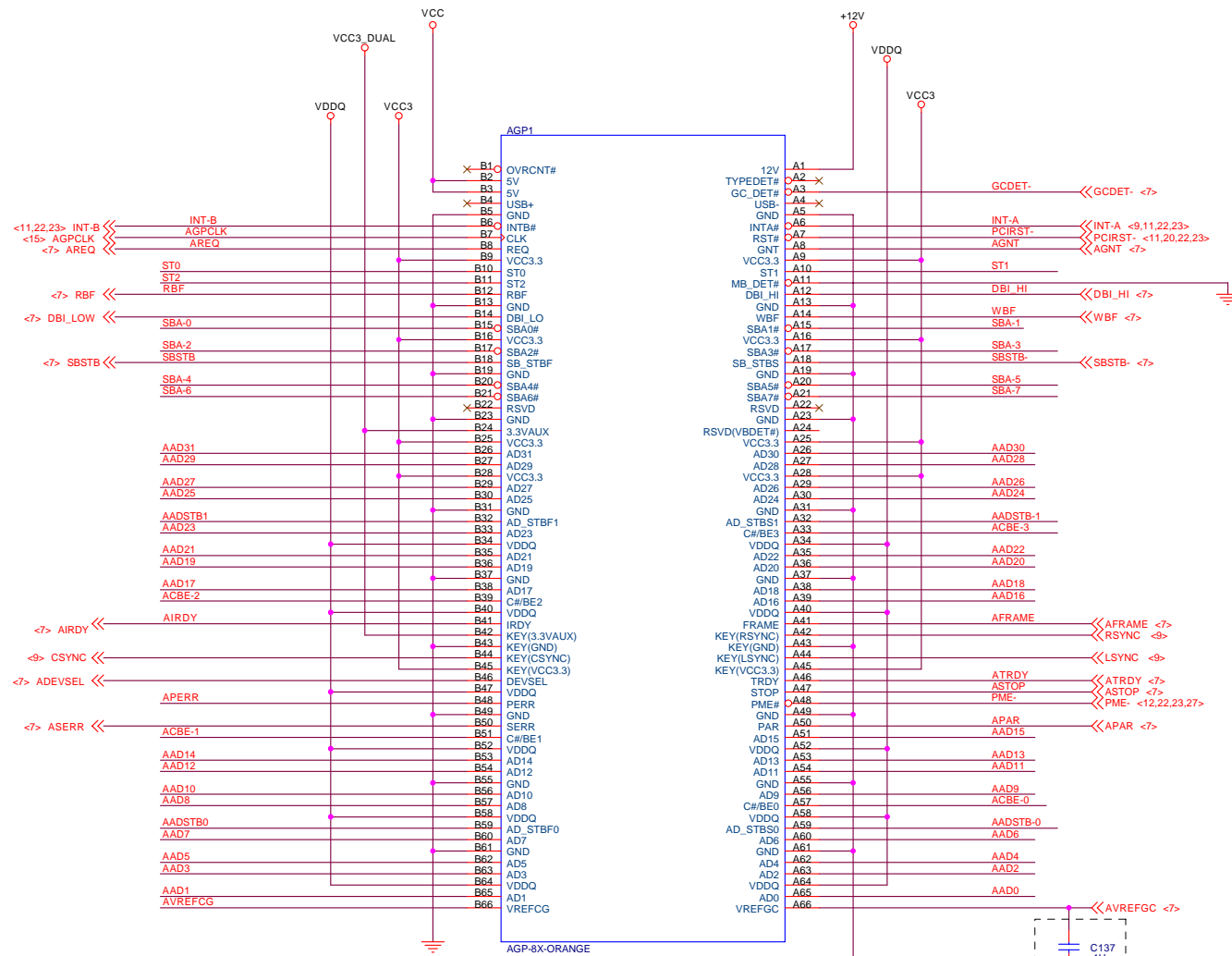
	SDR		DDR		
MD/DQM(/DQS)	LV-CMOS	D/10/-	SSTL-2	R _{in}	R _{tt}
MA/Control	LV-CMOS	1.0	SSTL-2	1.0	33
CS	LV-CMOS	0	SSTL-2	0	33
CKE	0 3.3V	0	0 2.5V	0	47

DMD[0..63] <<DMD[0..63] <8,17>
 DMA[0..14] <<DMA[0..14] <8,17>
 DDQM[0..7] <<DDQM[0..7] <8,17>
 DQS[0..7] <<DQS[0..7] <8,17>
 DCS[0..3] <<DCS[0..3] <8,17>

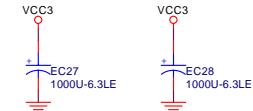


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
 0603 Package placed within 200mils of VTT Termination R-packs



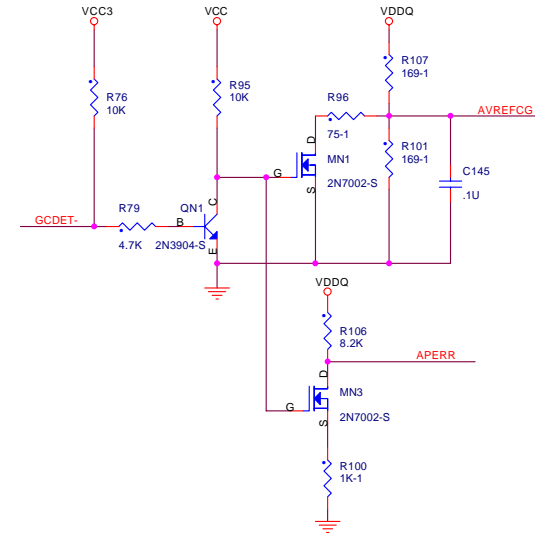


AGP CONNECTOR DECOUPLING
put CAP close to AGP slot each POWER PIN

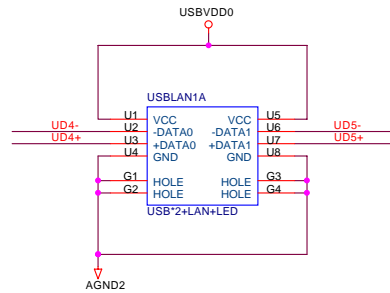
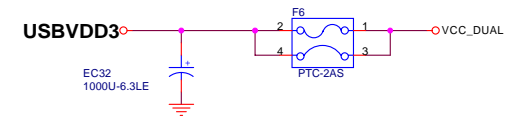
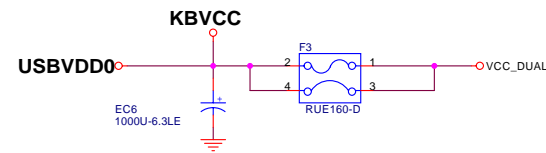


<7> SBA-[0..7] << SBA-[0..7]
<7> ST[0..2] << ST[0..2]
<7> ACBE-[0..3] << ACBE-[0..3]
<7> AAD[0..31] << AAD[0..31]
<7> AADSTB[0..1] << AADSTB[0..1]
<7> AADSTB-[0..1] << AADSTB-[0..1]

GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0
AVREFCG	0.35	0.75
APERR	0	1.5

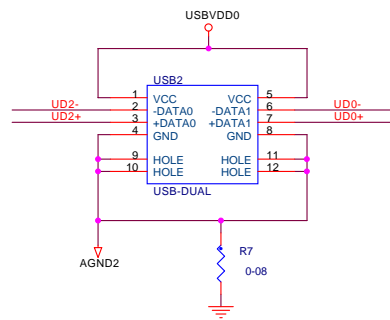


close to 660



UD5- <<UV5- <13>
UD5+ <<UV5+ <13>
UD4- <<UV4- <13>
UD4+ <<UV4+ <13>

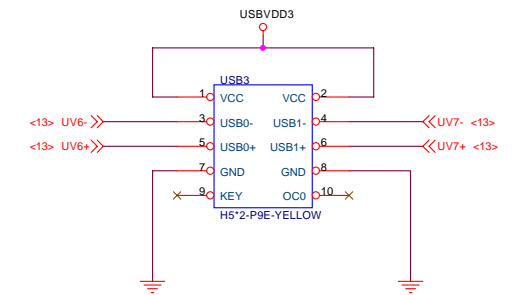
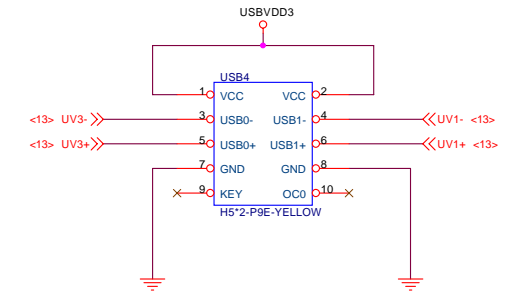
Close to USBLAN1 connector



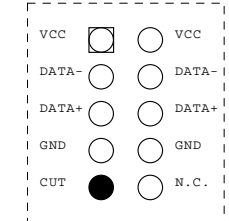
UD0- <<UV0- <13>
UD0+ <<UV0+ <13>
UD2- <<UV2- <13>
UD2+ <<UV2+ <13>

Close to USB1394A_J1 connector

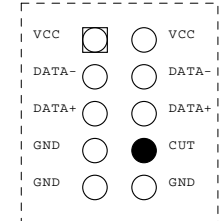
	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



Intel USB Header

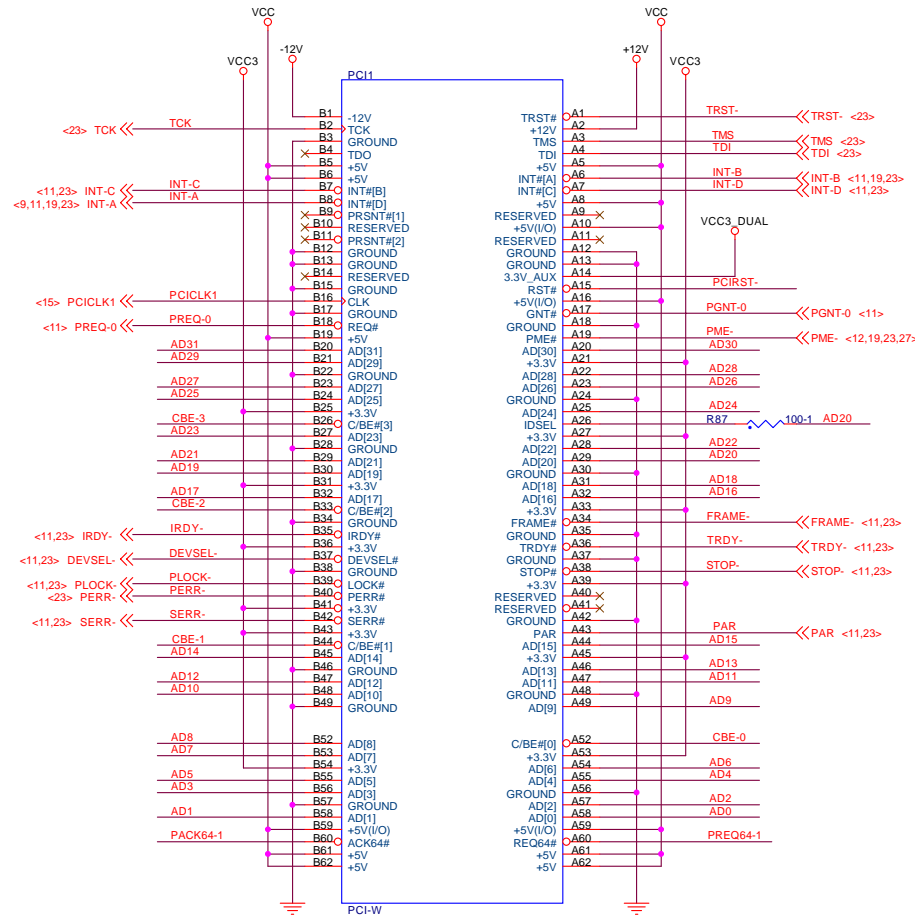


ACER USB Header

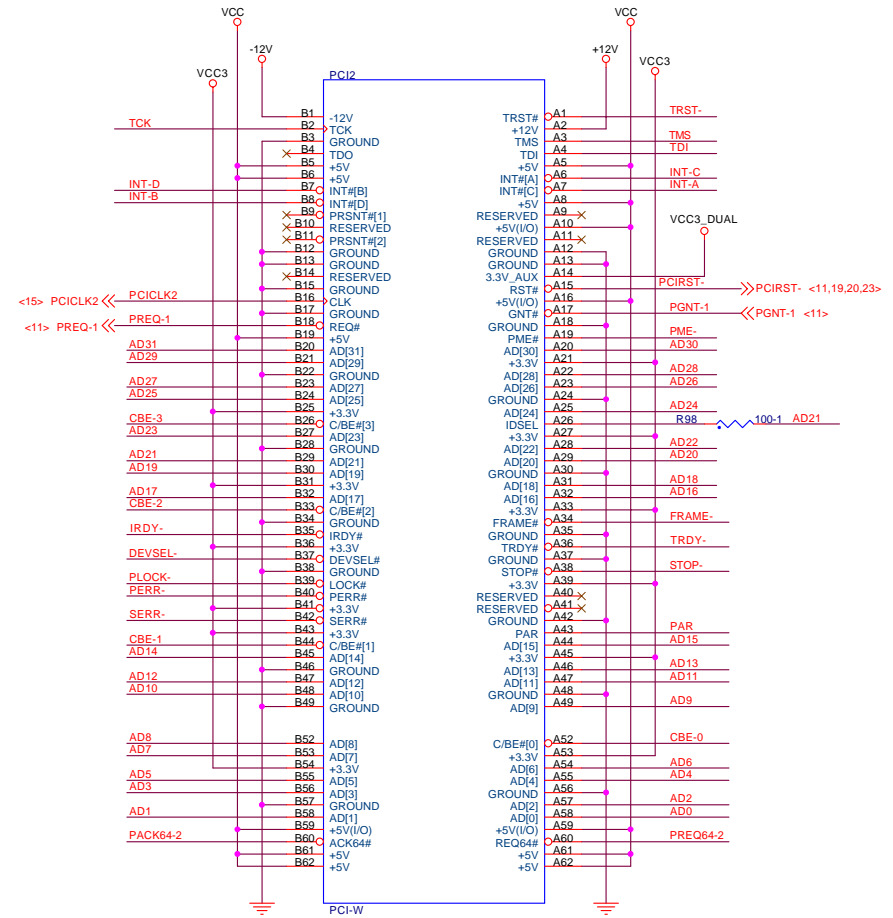


PCI Slot 1 & 2

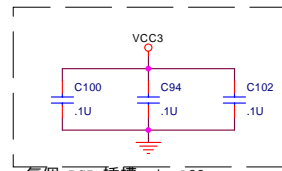
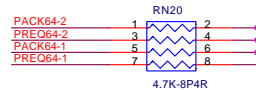
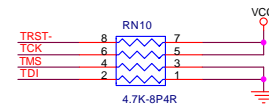
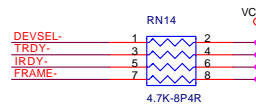
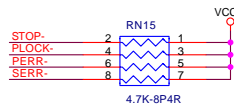
<11,23> CBE-[0..3] << CBE-[0..3]
<11,23> AD[0..31] << AD[0..31]



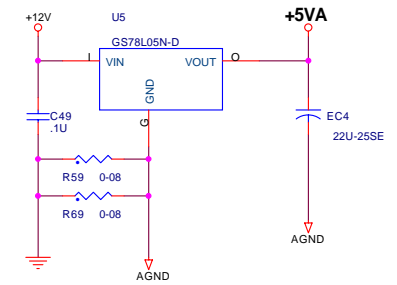
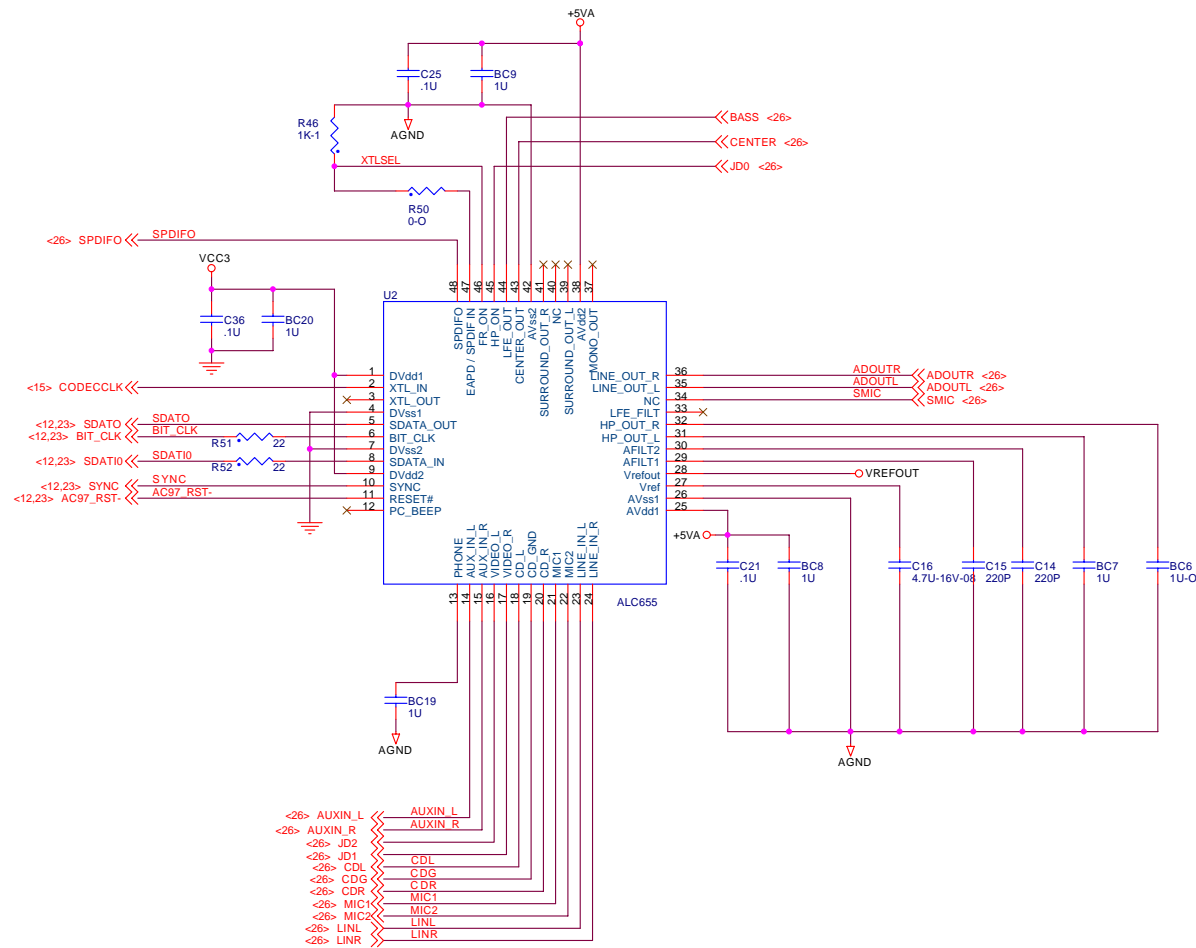
IDSEL=AD20
INT[B,C,D,A]

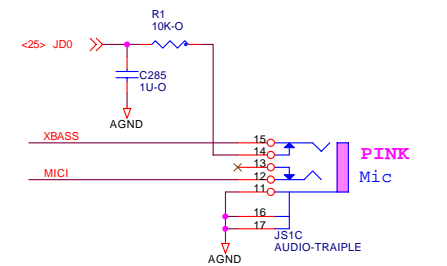
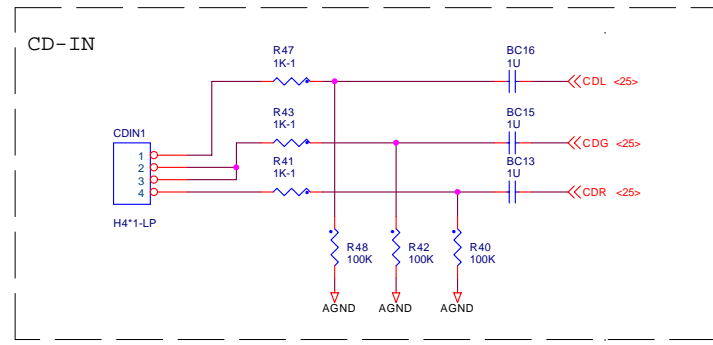
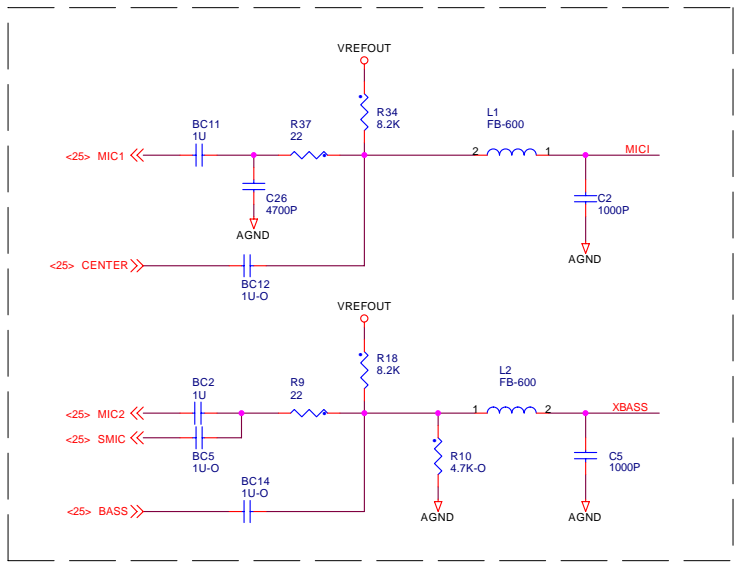
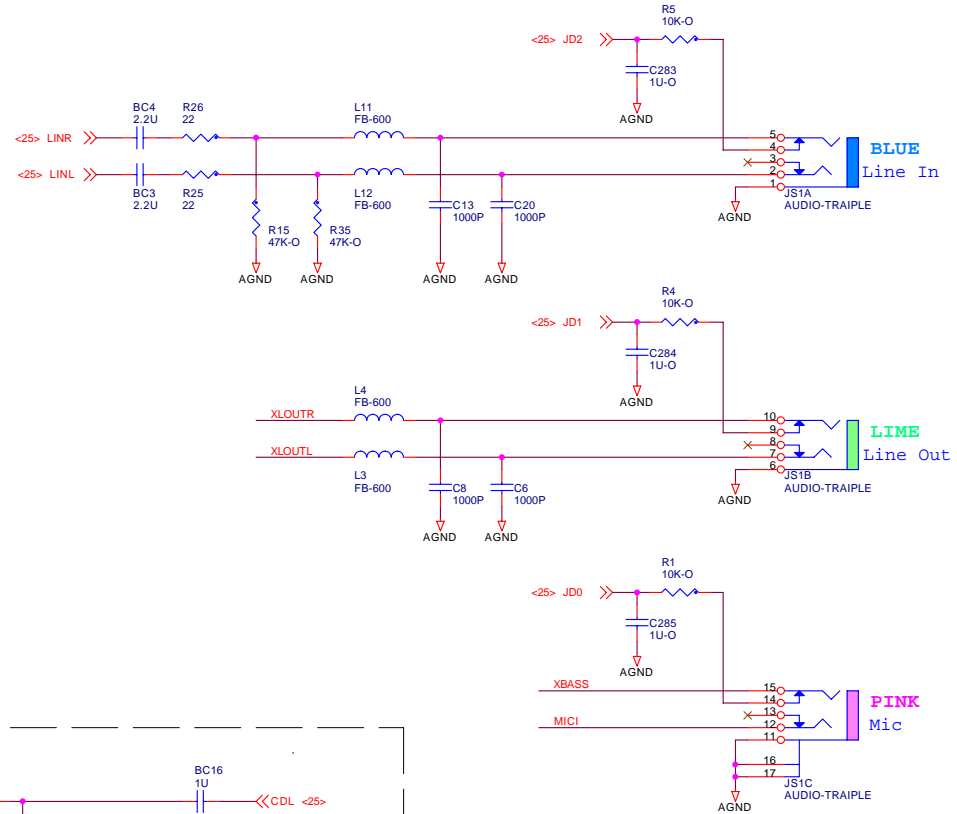
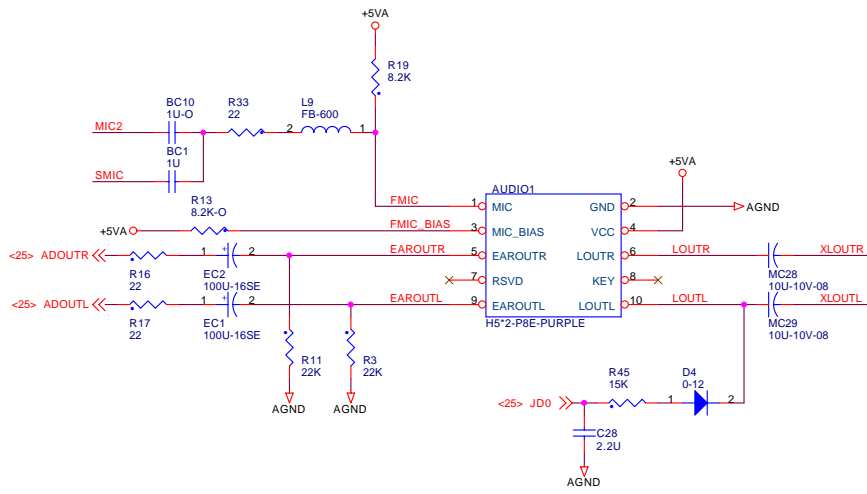


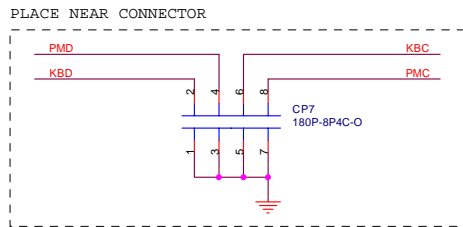
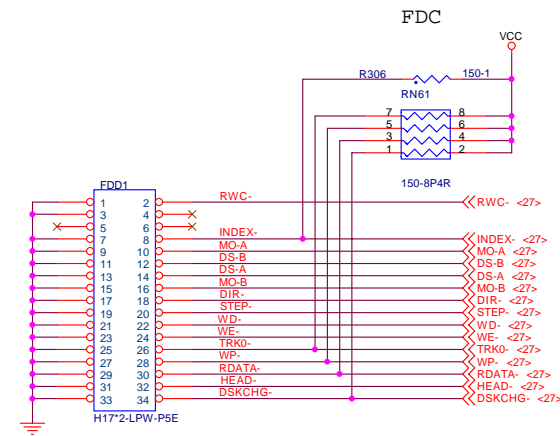
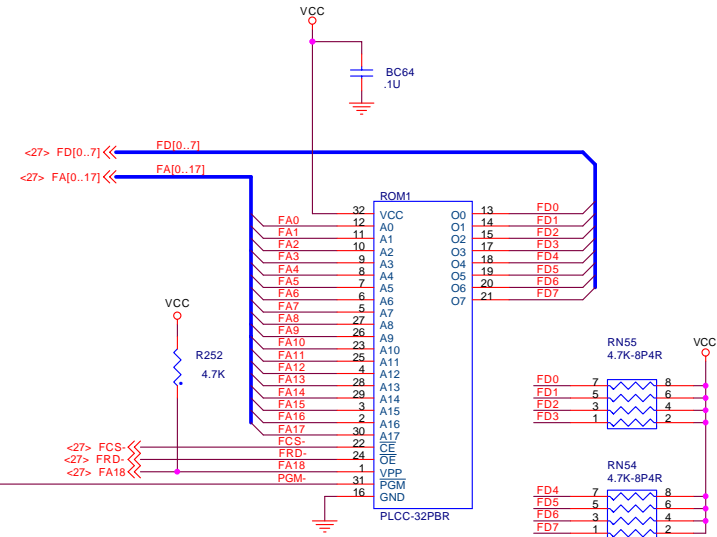
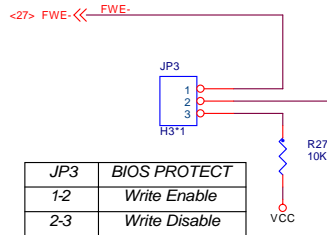
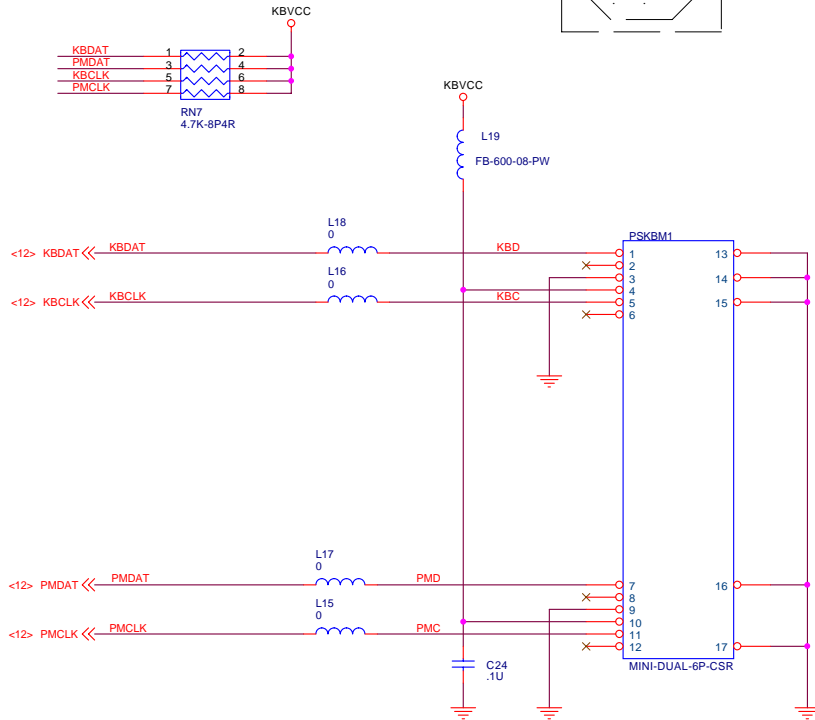
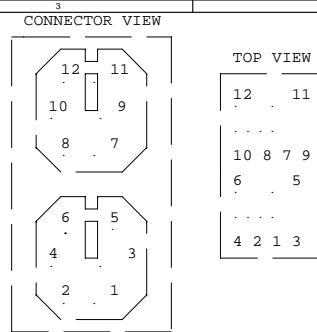
IDSEL=AD21
INT[C,D,A,B]

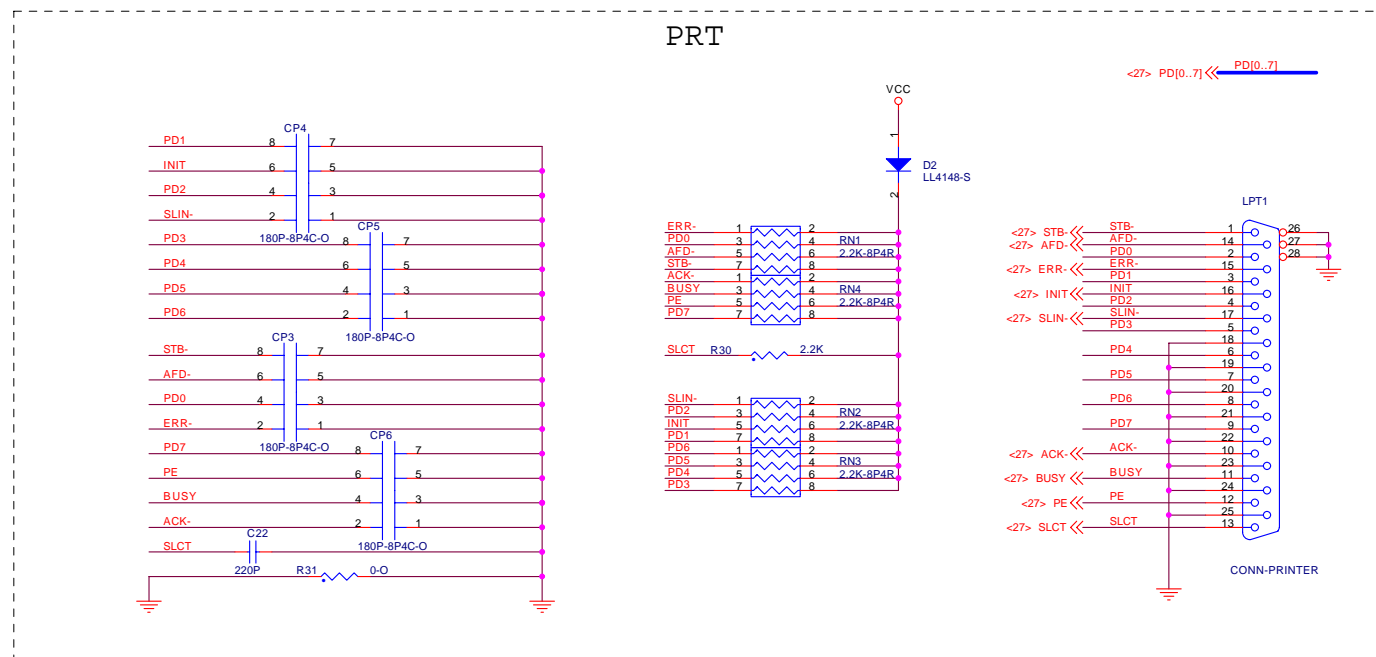
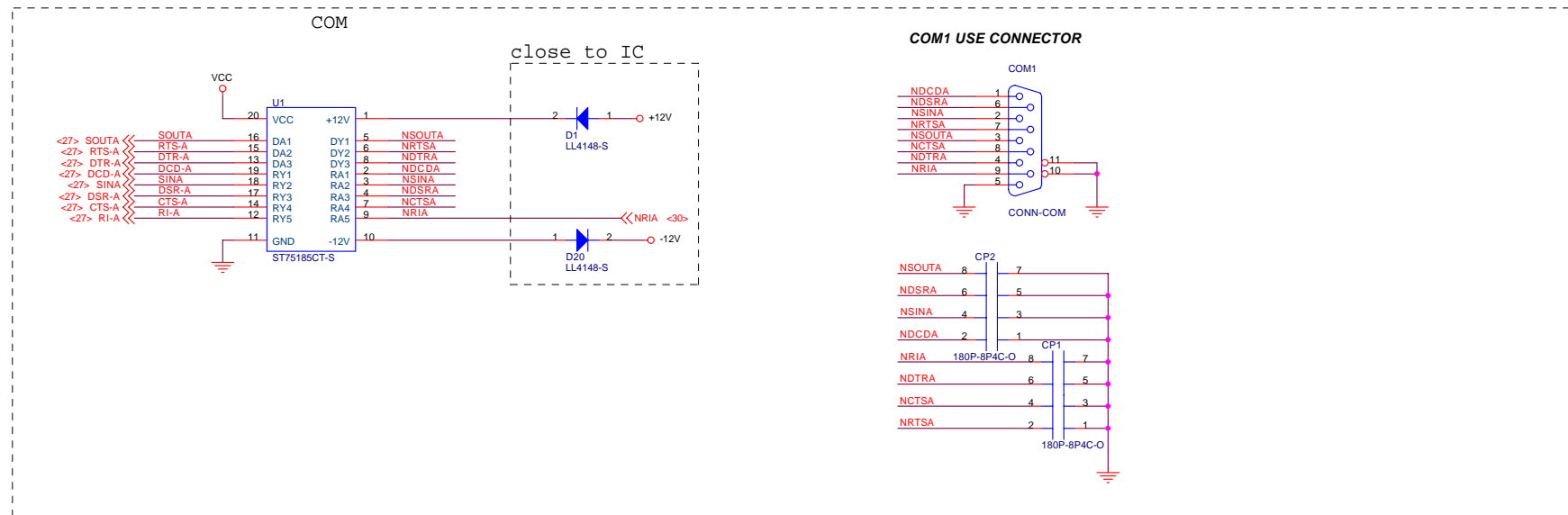


每個 PCI 插槽 pin A33
各放一顆

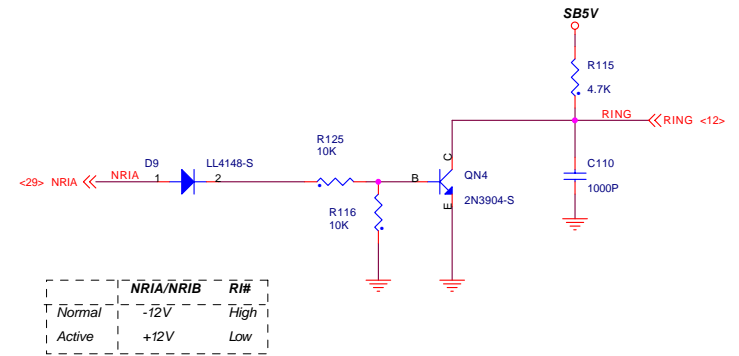
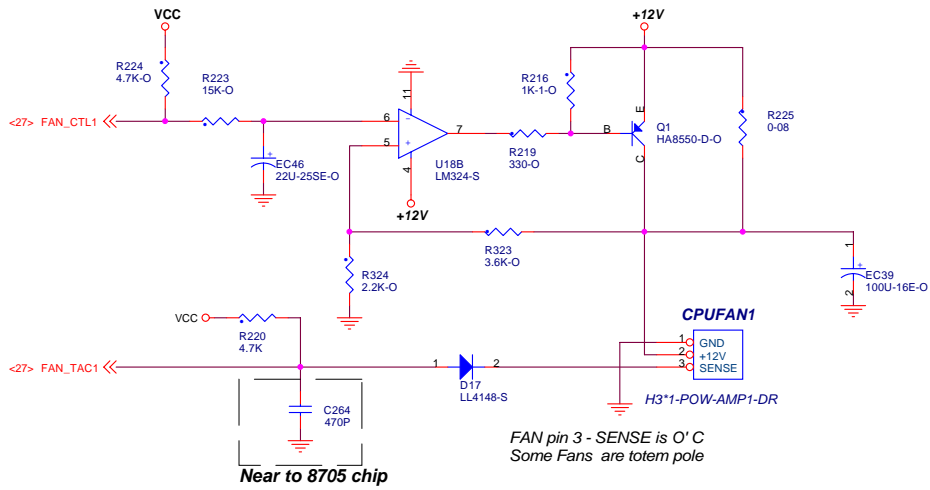






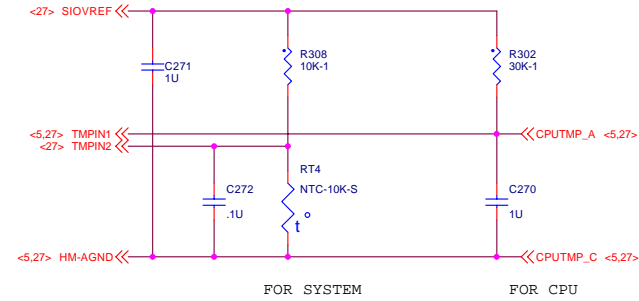


Layout :
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

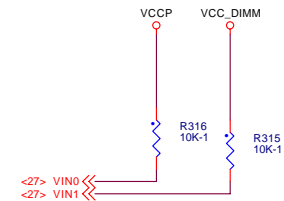


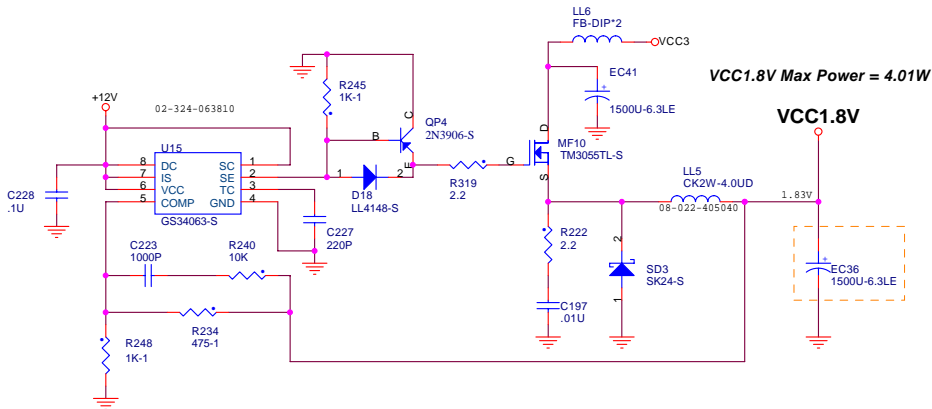
Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode



Voltage Monitor

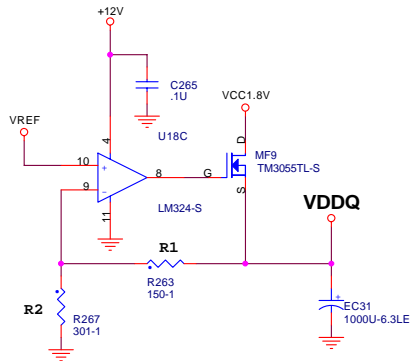




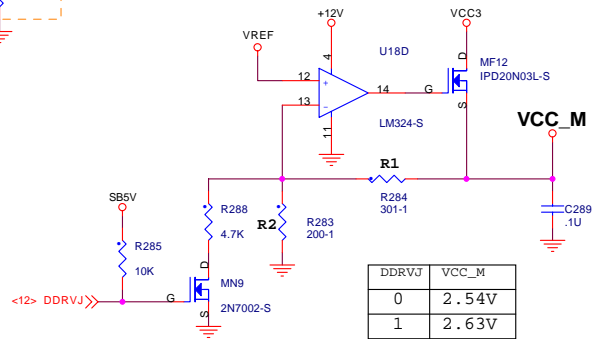
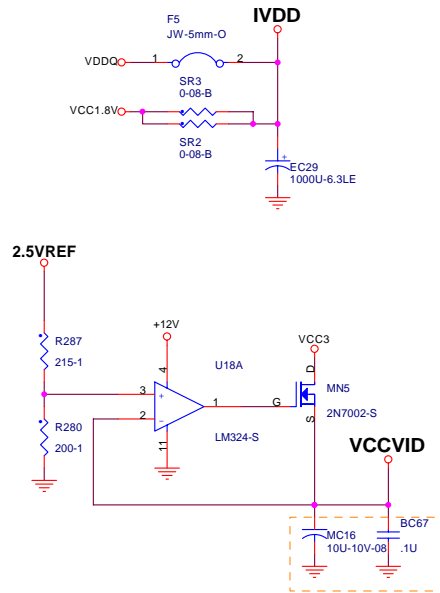
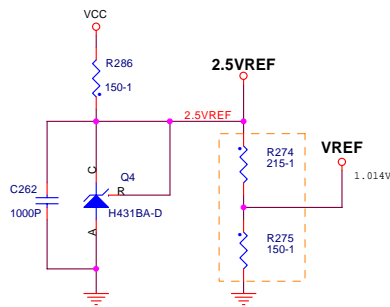
	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator
661FXLV	1.5V	1.8V	two regulator

	AUX_IVDD	SB1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator
661FXLV	1.5V	1.8V	two regulator

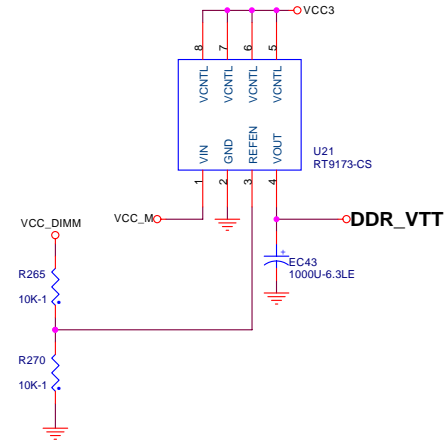
VCC1.5V Max Power = $0.3 \cdot (0.289 + 2.35) = 0.7917W$



$$V_o = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$



DDRVJ	VCC_M
0	2.54V
1	2.63V



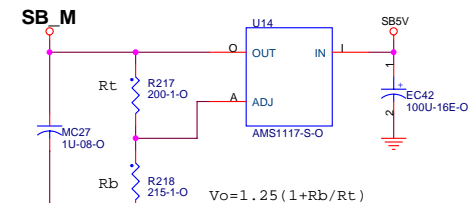
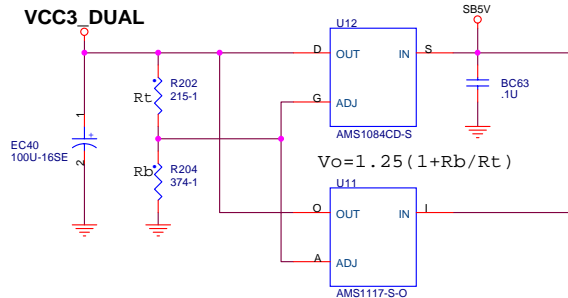
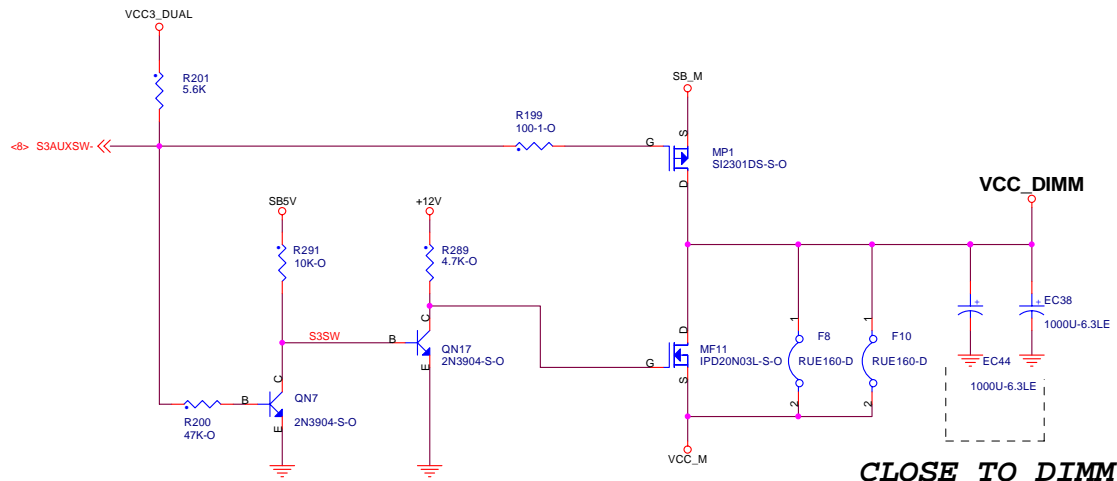
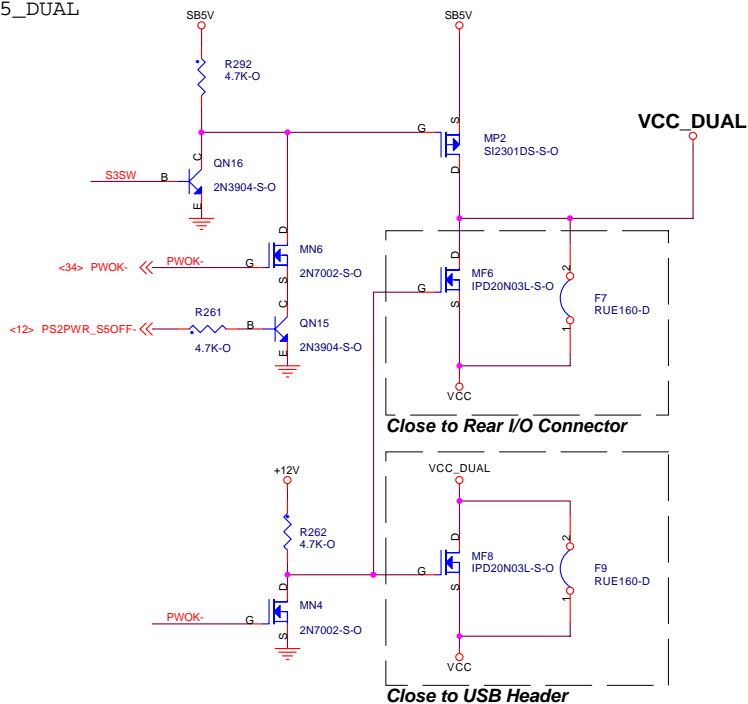
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

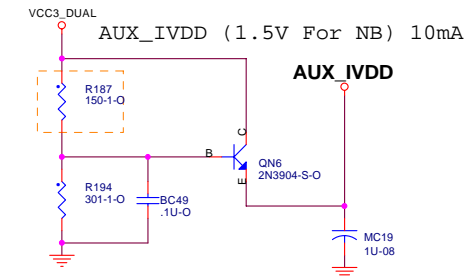
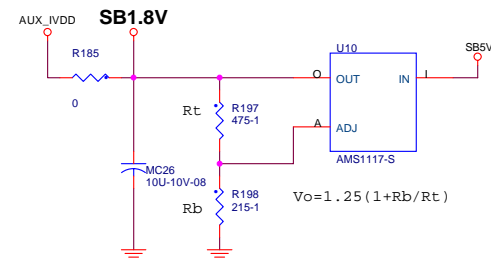
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER.(ADDITIONAL
500mA PER USB PORT)

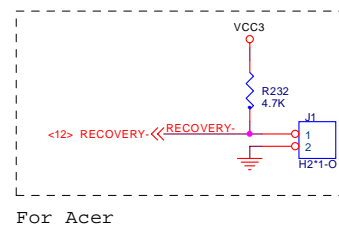
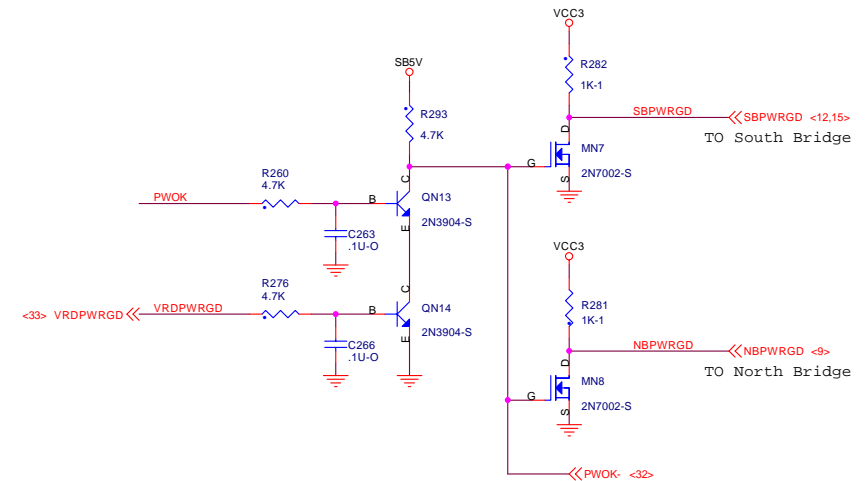
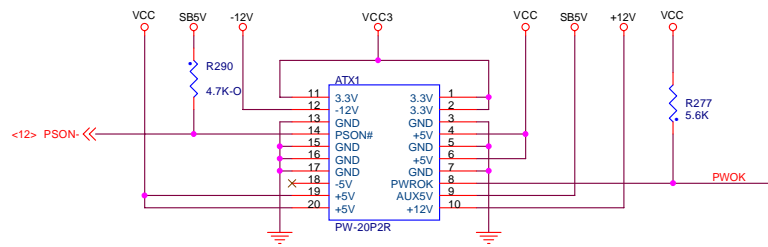
VCC3_DUAL & VCC5_DUAL



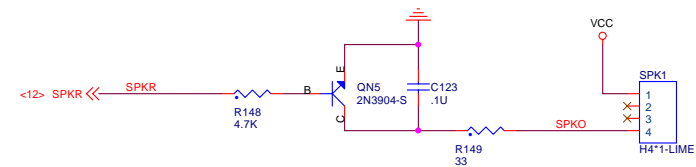
SB1.8V (For SB) 450mA



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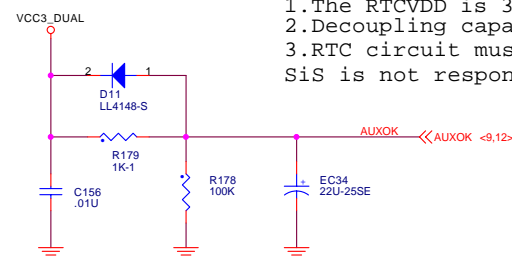
For Acer



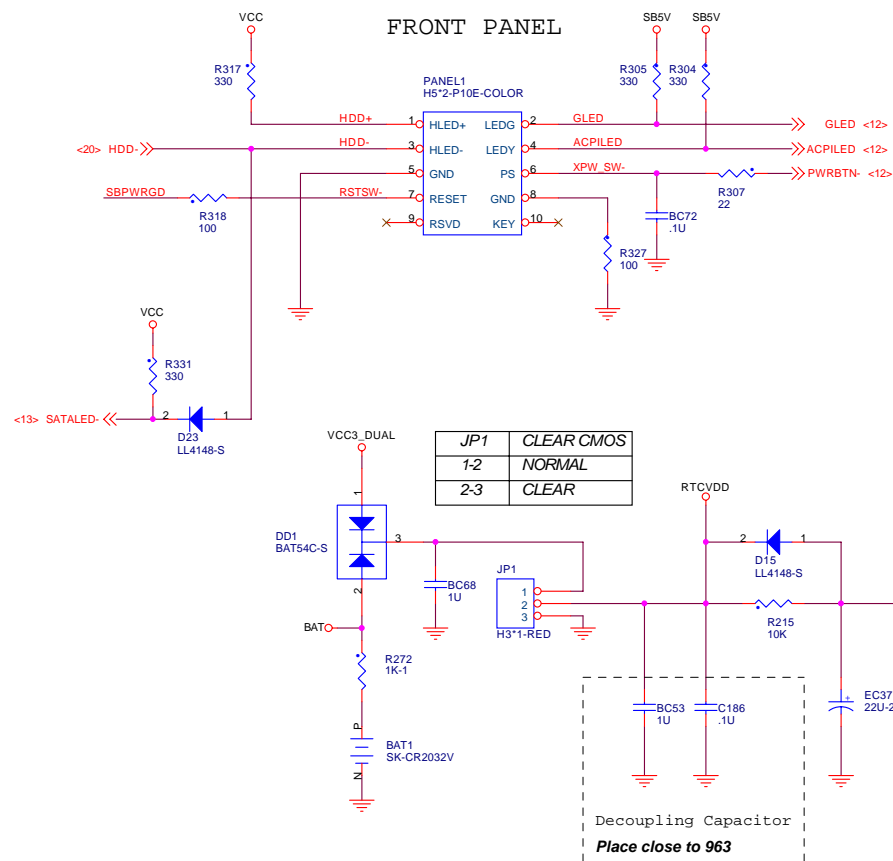
RTC

NOTE!

- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 635 RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.



FRONT PANEL



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